PC Board Layout Guidelines For LonWorks® Devices

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PC Board Layout Guidelines for LONWORKS® Devices

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[1] Introduction & Motivation

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[1.1] Why Are Networked Devices Different?

- **Increased Exposure to Real-World Disturbances**
  - Exposed Network Connectors Take ESD Hits
  - Power Mains Noise Feeds Through Devices to Network
  - Long Network Wiring Acts Like RF Receiving Antenna
- **Increased Visibility of Problems to End Users**
  - The More Useful A Network Is.....
    The More Obvious A Device Failure Is
  - Network Wiring Runs All Over.....
    So If You Generate EMI, You Will Interfere With Somebody
- **Note: LONWORKS Networks Are Only Different Because They Are Becoming So Popular.....We HAVE To Do Them Well!**

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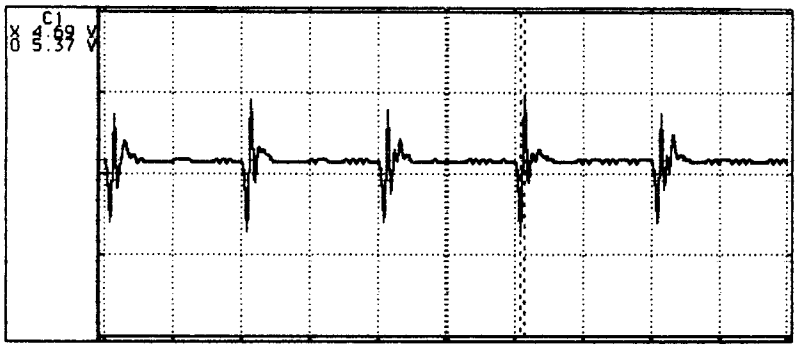
[1.2a] Noise Plots From PC Boards

- **A real example of poor bypassing**
  - Several bulk capacitors are connected to ICs with narrow, separated, 2cm long traces
  - Test conditions: Vdd-Vss at Neuron 3150 Chip, 5MHz clock, 400mV/vertical division, 100nsec/horizontal division.

Vnoise = 0.68V



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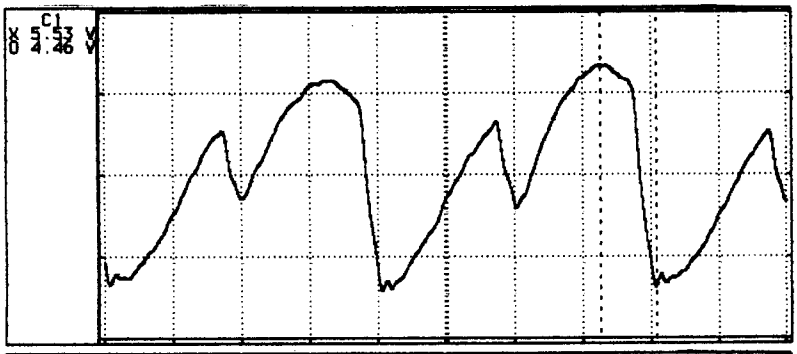
[1.2b] Noise Plots From PC Boards

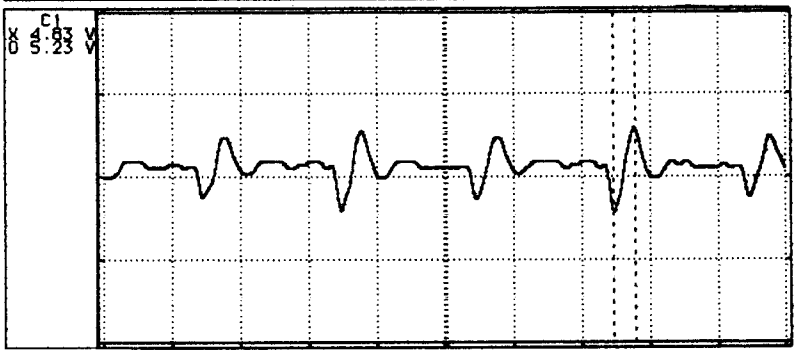
No
bypass capacitors

Vnoise=1.1V



2.2µF bulk
bypass capacitor

Vnoise=0.4V



- Test conditions: Vdd-Vss at Neuron 3150 Chip, 2-layer board, 0.5m power cable, 5MHz clock, 400mV/vertical div, 100nsec/horizontal div

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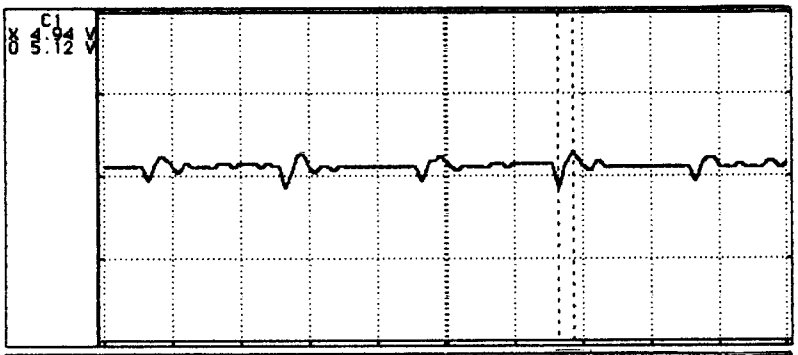
[1.2c] Noise Plots From PC Boards

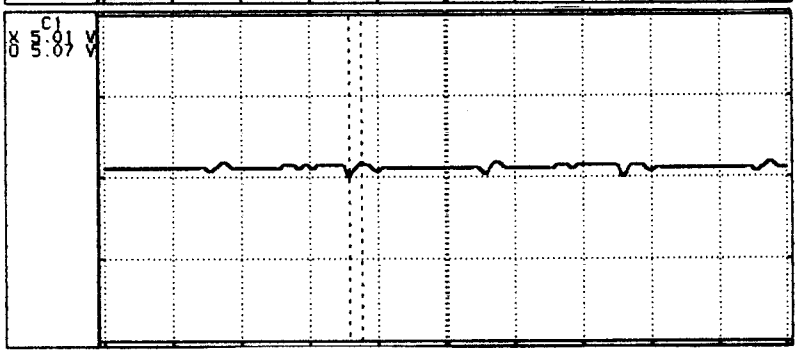
2.2µF bulk +
0.1µF disc
bypass capacitors

Vnoise=0.18V



2.2µF bulk +
0.1µF surface-mount
bypass capacitors

Vnoise=0.06V



- **Test conditions: Vdd-Vss at Neuron 3150 Chip, 2-layer board, 0.5m power cable, 5MHz clock, 400mV/vertical div, 100nsec/horizontal div**

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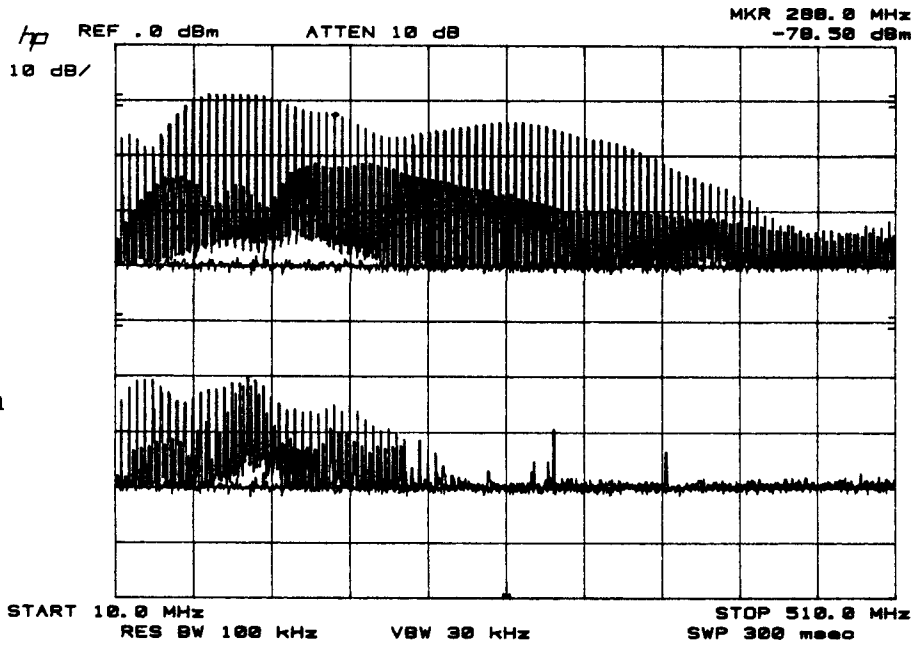
[1.2d] Noise Plots From PC Boards

- Frequency content at Vdd-Vss pins of Neuron Chip

Bad 2-layer design

Good 2-layer design



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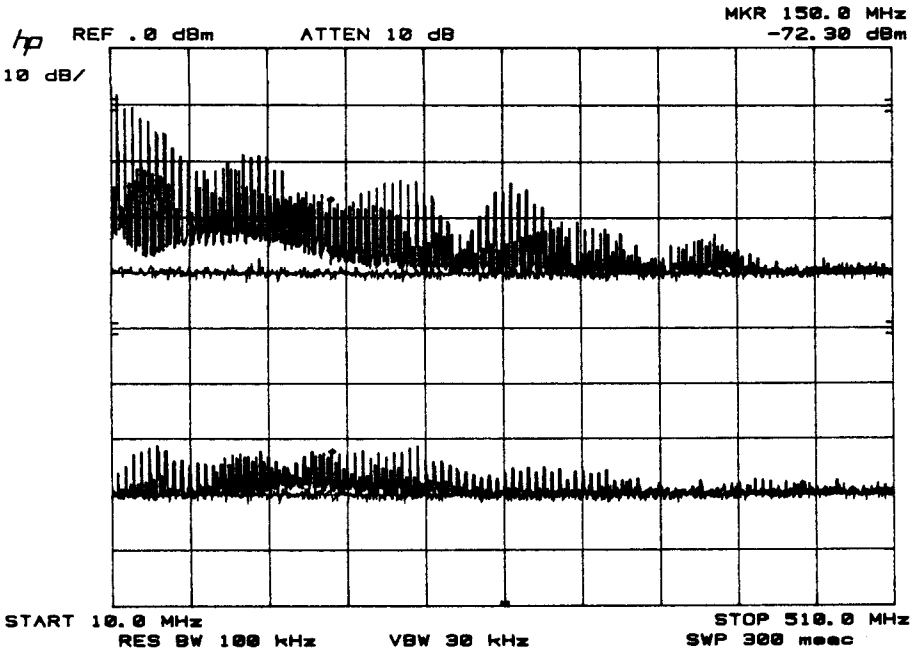
[1.2e] Noise Plots From PC Boards

- Frequency content at Vdd-Vss pins of Neuron Chip

Bad 4-layer design

Good 4-layer design



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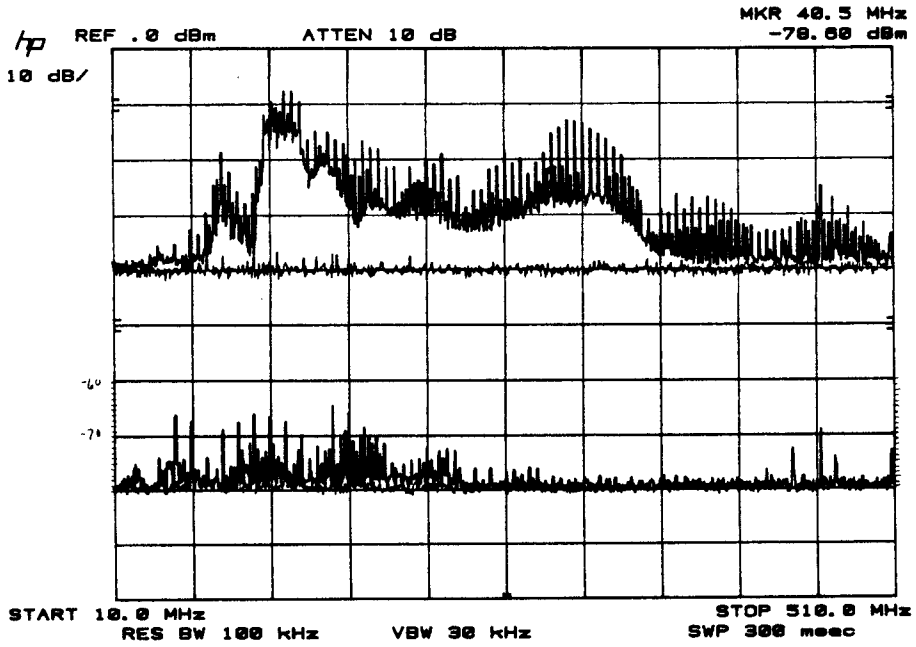
[1.2f] Noise Plots From PC Boards

- Radiated emissions using sniffer probe at 30cm

Bad 2-layer design

Good 2-layer design



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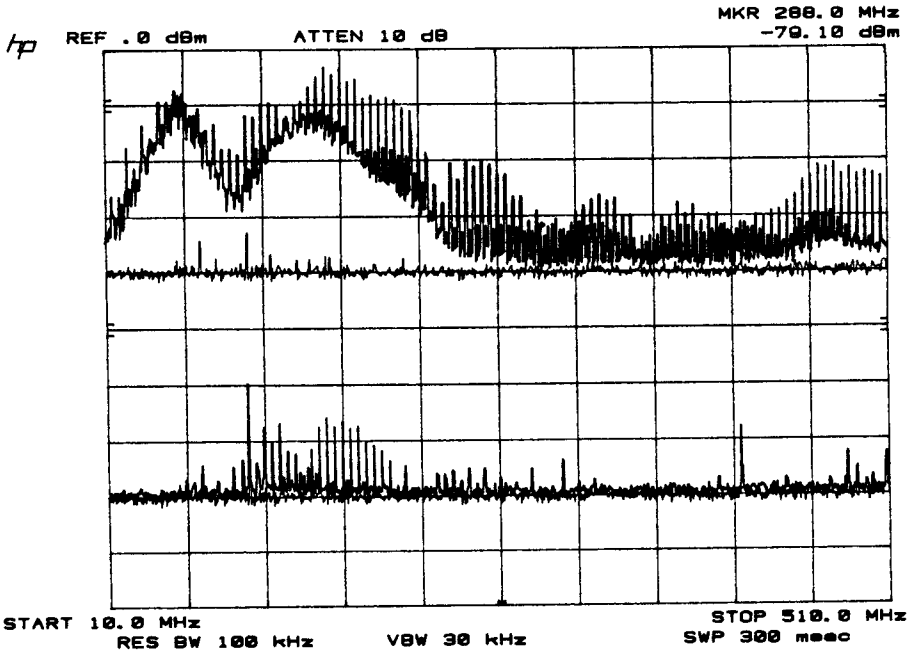
[1.2g] Noise Plots From PC Boards

- Radiated emissions using sniffer probe at 30cm

Bad 4-layer design

Good 4-layer design



[1.3] Some Customer Problems.....

- **Customer With Neuron® Chip Burnup Problems in "Lightning Country"**
  - PROBLEM: Neuron Chips were resetting & latching up.
  - DEBUG: Review of PCB artwork showed inadequate grouding & bypassing. "Top Hat" rework improved immunity of test PCB.
  - SOLUTION: Revised PCB grounding, bypassing, Reset trace routing.
- **Customer With Both Sides Of A Custom Router Damaged By ESD**
  - PROBLEM: Both sides of a TP Control Module-based custom router went Applicationless from an ESD hit to one side's network connector.
  - DEBUG: Review of motherboard & enclosure design showed that the TP Control Modules had no P2 standoff ground connection.
  - SOLUTION: Add P2 standoff as per Control Module User's Guide.
- **Customer With Simple Power Line Devices Taking Over The Network**
  - PROBLEM: Simple 3120 + PLT-20 Nodes had their comm parameters consistently scrambled by Power Line transients. This resulted in the PLT-20 continuously blabbing onto the Power Line.
  - DEBUG: Review of PCB & metal enclosure showed no star ground.
  - SOLUTION: Shoulder washers on 3 of 4 standoffs made a star ground.

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[1.4] How Echelon Tests Transceivers

- **Design & Fabricate Initial PC Boards For Testing**
  - Echelon uses 2-layer PCBs whenever possible. If EMI problems are anticipated, start w/ best 2-layer design, & add inner layers as contingency
  - Echelon uses a PCB Milling Machine (LPKF) for quick-turn & experiments
  - Echelon also builds large "Node Farms" and wire tables to test full-size, fully-loaded networks in different configurations
- **Do Initial Transient & Reliability Testing**
  - "STRIFE" Testing: 10C/minute thermal cycling, 10-15C beyond operating temperature range, including power cycling.
  - IEC801-2 ESD Testing: ± 15kV air discharge, ±8kV contact discharge
  - IEC801-3 RF Susceptibility Testing at local test lab's Anechoic Chamber
  - IEC801-4 Burst Testing w/ network cable clamp & into power cord
  - IEC801-5 Surge Testing into network cable & into power cord
- **Do Additional Environmental Testing**
  - Humidity, Supersoak, Shock, Vibration & Altitude testing done at a local environmental test lab

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[1.5] Useful Tricks & Techniques You Will Learn Today

- **Techniques for simplified EMI debugging in your lab**
- **When to use a Neuron 3150B1 Chip to help your EMI**
- **ESD debugging techniques, including the "Top Hat Rework" and how to make a simple fiberoptic probe**
- **How to design your PCB using the "Star Ground" concept..... .....even if you are using a plastic enclosure**
- **What to look for in an Undervoltage Reset part..... .....and when you can use just the B1 Neuron Chip's internal LVI**
- **And more.....**

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[2] Detailed PCB Design Considerations

[2.1] An Example Layout: Neuron 3120 Chip + FTT-10

[2.2] PCB Design From The Ground Up: Star Grounding

[2.3] ESD & EMI Keepout Areas

[2.4] Power Distribution & Vcc Decoupling

[2.5] Reset Signal Conditioning & LVI Issues

[2.6] High-Speed Signal Routing Issues

[2.7] Other Layout Considerations

[2.8] Other Design Examples With the Neuron 3150 Chip

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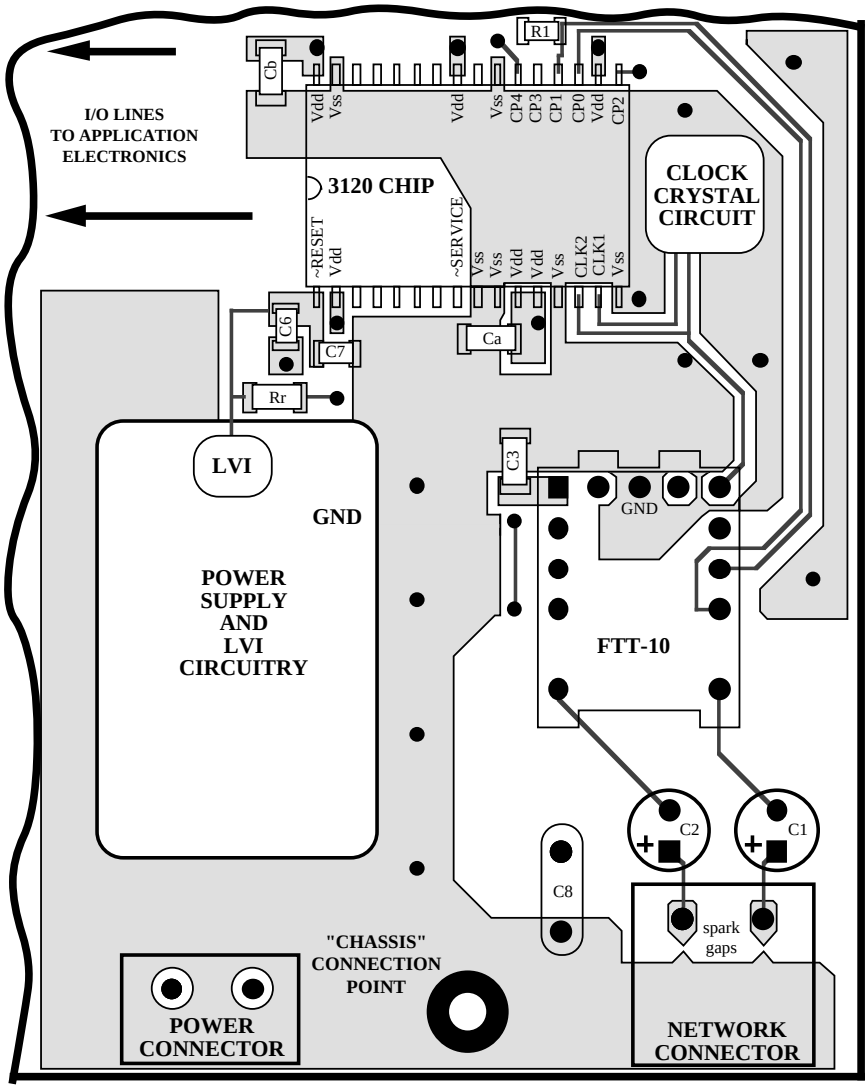
[2.1a] Example Layout: Neuron 3120 Chip + FTT-10 (Component Side, Top View)



- **Good Star Ground Layout (connectors are together)**
- **Low Inductance Ground Under Neuron 3120 Chip on Comp. Side**
- **Multiple Vcc Decoupling Caps around Neuron 3120 Chip & FTT-10**
- **Clock Traces Are On Comp. Side & Guarded With Ground**
- **Reset Pin of Neuron 3120 Chip is Decoupled Well**
- **FTT-10 Transceiver Vcc is Decoupled Well**
- **(Note: Spark Gaps Are For FTT-10 Transceiver Only)**

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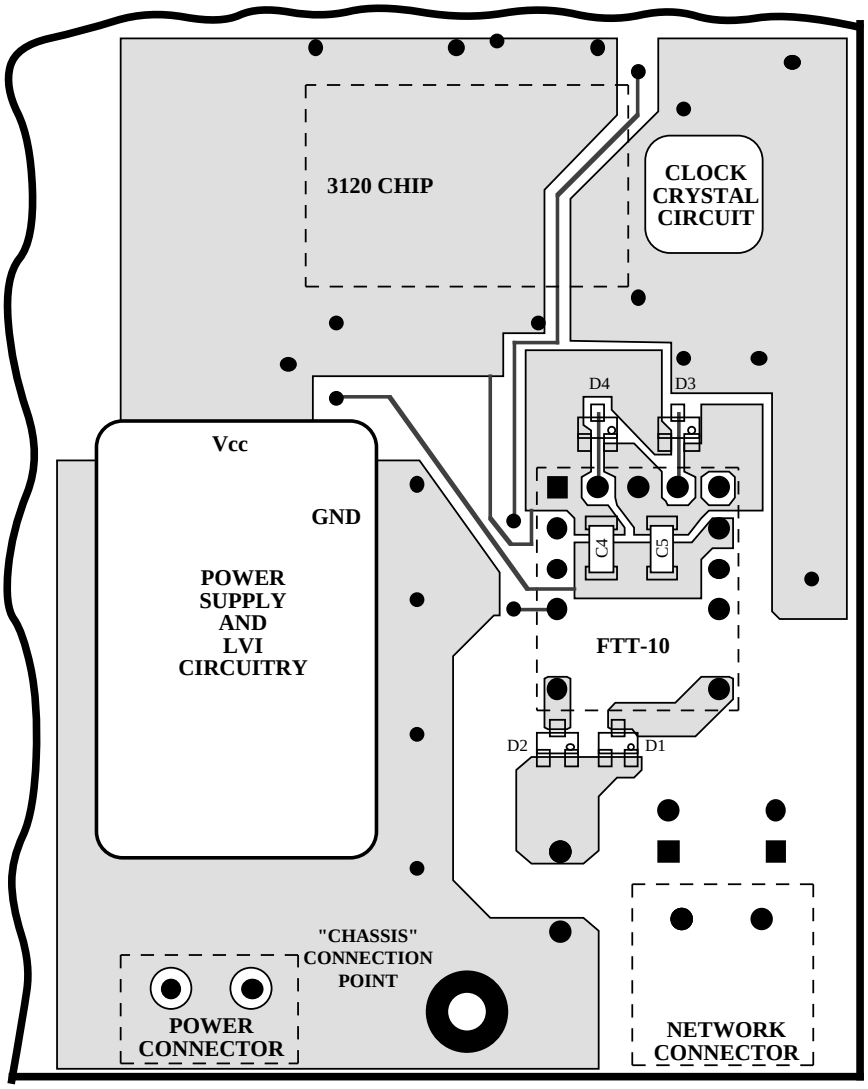
[2.1b] Example Layout: Neuron 3120 Chip + FTT-10 (Solder Side, X-Ray View)



- **Solder Side Guarding of Clock Traces**
- **Low Inductance Decoupling of Reset Pin on FTT-10**
- **Vcc Filtering For FTT-10 (skinny Vcc trace & good decoupling cap)**
- **ESD Keepout Area Around Network Traces**
- **(Note: Thermal reliefs for connections to ground planes and Vcc planes are not shown.)**

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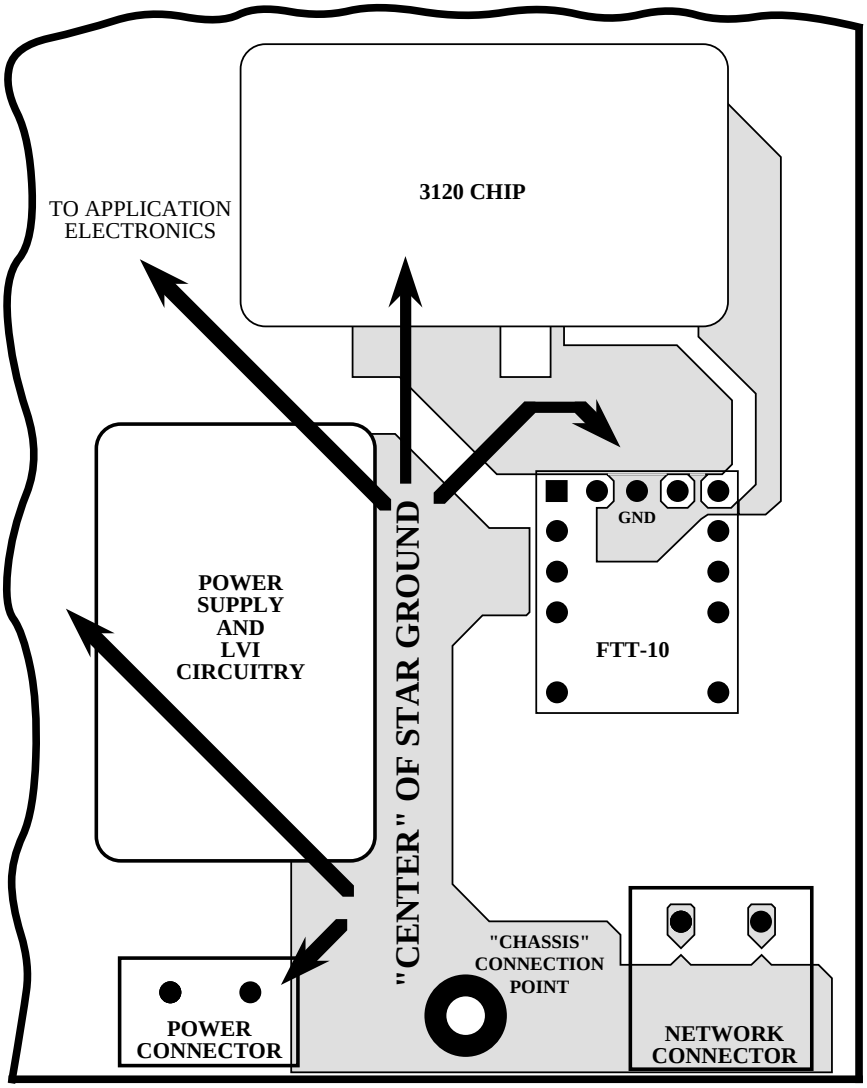
[2.2a] Design From The Ground Up: Star Grounding



- **Low Inductance (wide) Center of the Star Ground**
- **All Sensitive Circuitry Is Kept Away From Star Center**
- **Each Function Block Shares Minimal Ground Impedance with Other Function Blocks**
- **All Transient Entry & Exit Points Are Near Star Center:**
  - Network Connector, Power Connector and Chassis Ground Connection Point are all together
- **"Count Squares" to Minimize Inductance**
  - A trace with a 5:1 (L:W) aspect ratio counts as 5 squares
  - Try to keep ≤ 5-10 squares in ground connections

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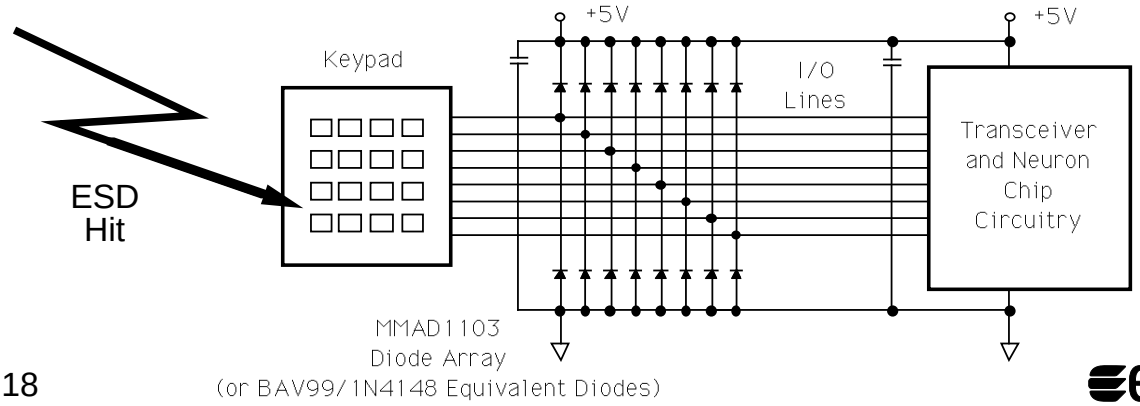
[2.2b] Design From The Ground Up: Star Grounding

- **All Transient Entry & Exit Points Should Be Near Star Center**
  - Network Connector, Power Connector, Chassis GND Standoff
  - Display or Keyboard Connectors (if they are exposed to ESD hits)
- **Transient Currents MUST Be Kept Away From Circuitry**
  - Keep transient currents away from Neuron Chip (EEPROM errors, latchup)
  - Keep transient currents away from sensitive analog circuitry
- **Use ESD Clamp Diodes On Sensitive Lines Exposed To ESD Hits**
  - Typical Example: Keypad Scanning with I/O Lines



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[2.3] ESD & EMI Keepout Areas

- **ESD Keepout Areas**
  - Keep sensitive traces away from the Network connector
  - ESD "Clearance" arcs can jump ≥ 0.5" through the air
  - ESD "Creepage" arcs can jump ≥ 1.5" across surfaces
  - Use Ground Guarding to shunt creepage arcs to Star Center
  - Spark Gaps provide reasonably-controlled shunt path
- **EMI Keepout Areas**
  - Keep RF "Hot" signals away from Network, Power connectors
  - Usually best to route RF hot signals on component side of PC board, and use full ground guarding
  - Use some ground guarding around network & power connectors
  - Keep magnetic field noise sources (like DC-DC converter inductors) away from transceiver transformer

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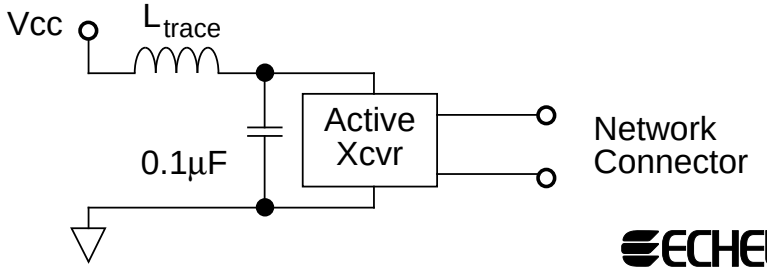
[2.4] Power Distribution & Vcc Decoupling

- **Wide Vcc distribution planes are less important on PC Boards that have good grounding and decoupling**
- **Use 0.1μF SMT caps on component side of PCB, directly adjacent to each IC's Vcc pin wherever possible**
- **Use 3-4 caps around the Neuron Chip for good decoupling**
- **Use "Quiet Vcc" trick with active transceivers for low EMI:**
  - **Use a skinny Vcc trace to the active transceiver, and decouple the transceiver's Vcc pin well**
  - **This LC filter quiets the transceiver's Vcc supply, which quiets the RF noise that is coupled onto the network wiring**

Note: Trace Inductance is about 10-20nH per inch



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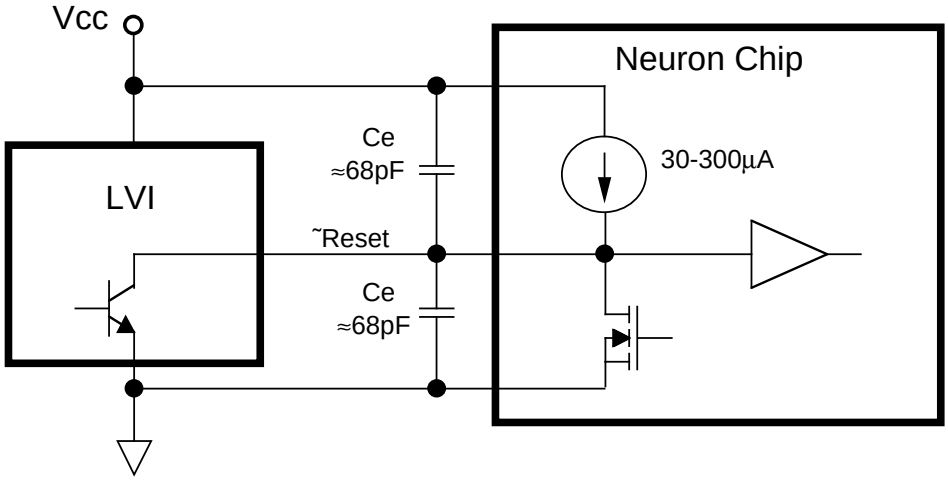
[2.5a] Reset Conditioning & LVI Issues

- **Undervoltage Reset Part Is NOT OPTIONAL**
- **Neuron Chips Must Have Reliable LVI To Prevent EEPROM Corruption**
  - LVI = "Low Voltage Interrupt" (asserts ˜Reset when Vcc is low)

MC34064
MC34164
MC33064
MC33164
DS1233-5
DS1233-10



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[2.5b] Reset Conditioning & LVI Issues

- **The ˜Reset line is a high-impedance, shared line**
  - Use Ce caps for decoupling of ˜Reset line (Ce ≤ 250pF total)
  - Keep the ˜Reset line short, and guard with ground as much as possible
  - Buffer the ˜Reset line if it has to be routed off-board
  - Open Collector or Open Drain LVI output is REQUIRED
  - If you have an existing node design with a non-open collector LVI, you must add a 5kΩ isolation resistor (cf: MAX70x data sheet)
- **External LVI is a special kind of circuit:**
  - Reliable assertion of ˜Reset guaranteed for Vcc ≥ 1.5V (so LVI must be connected to Neuron Chip ˜Reset pin w/o buffering)
  - Pulse-Stretching LVI needed for FTT-10, Flash memory
  - Note: when using an LVI, the old diode-capacitor delay circuit on the ˜Reset line is not needed
- **Internal LVI in 2nd generation Neuron Chips (3120B1, 3150B1) can be used if:**
  - The Neuron Chip is guaranteed to start up correctly on power-up using only its internal LVI circuit (consult Motorola & Toshiba)
  - Other external circuitry can tolerate a low LVI trip point (3V-4V range)..... Be sure to check your external memory operating voltage range!
  - A pulse-stretching LVI is not needed

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[2.6] High-Speed Signal Routing Issues

- **High-speed signals (clocks, memory bus lines, etc.) must be guarded from external metal surfaces**
  - **See Section 3.2 about leakage capacitance management**
  - **As much as possible, keep fast signal traces short, on the component side of the board, and guarded with ground**
    - The spacing from the component side of the board to the outside surfaces of the enclosure is usually greater than the spacing from the solder side of the board, so it is easier to guard component side traces
  - **Do not route fast signals over cables to other assemblies**
    - Do not route fast clock lines over cables
    - Use decoded latches to transfer memory-mapped I/O over cables.....never route the memory bus over a cable!
- **Use slower clocks where possible (5MHz is quieter than 10MHz)**

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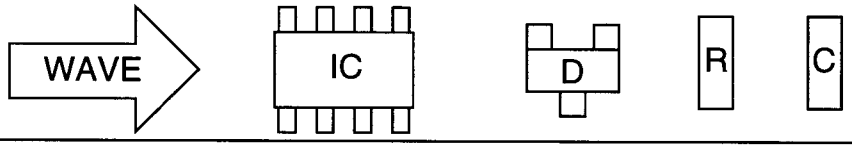
[2.7] Other Layout Considerations

- **TPT Transceiver Considerations (see the TPT User's Guide):**
  - **The CP lines must be short, low capacitance, guarded, and symmetric**
    - Clear out any inner layer ground or Vcc planes under CP lines
    - Use opposite-side ground guarding with ≤ 25% crosshatching
    - Keep CP line connections to TPT short & symmetric
- **Manufacturability Considerations**
  - **Consult your manufacturing department early for board reviews**
    - One ICT test point per net, panelization considerations, etc.
  - **Special considerations for SMT + through-hole designs:**
    - SMT parts on solder side must have correct orientations in order to be compatible with the solder wave direction
    - In general, no VLSI and no fine-pitch (<0.050") parts are allowed on the wave solder side of the board



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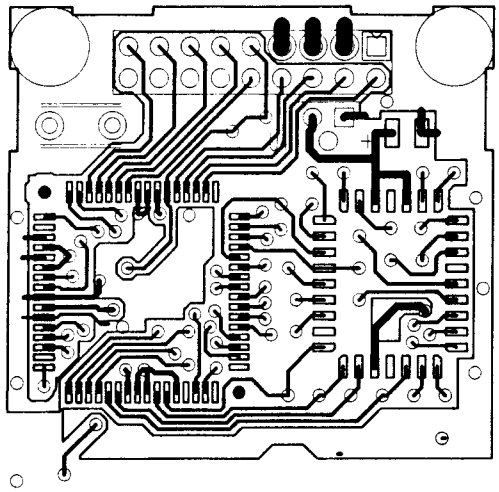
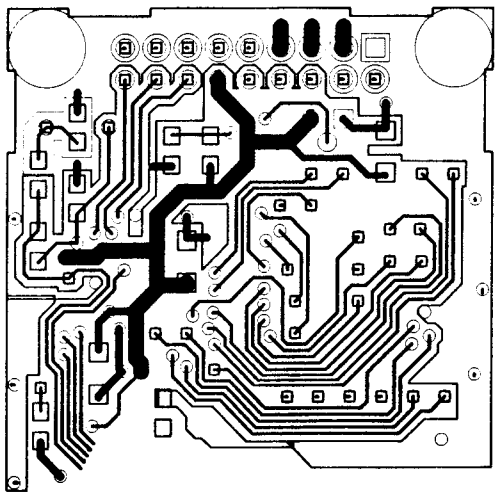
[2.8a] Other Design Examples w/ Neuron 3150 Chip

- **Core Circuit from TP/FT-10 Control Module (2-layer, 5MHz device)**

COMPONENT SIDE



SOLDER SIDE



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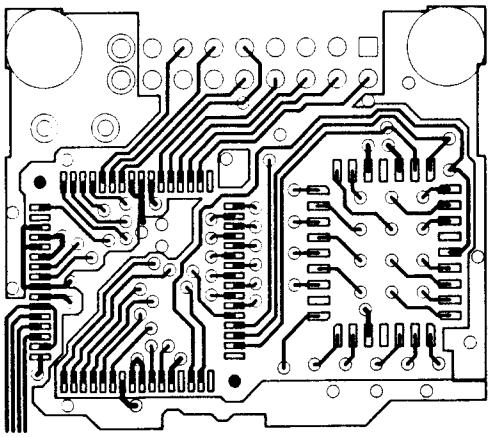
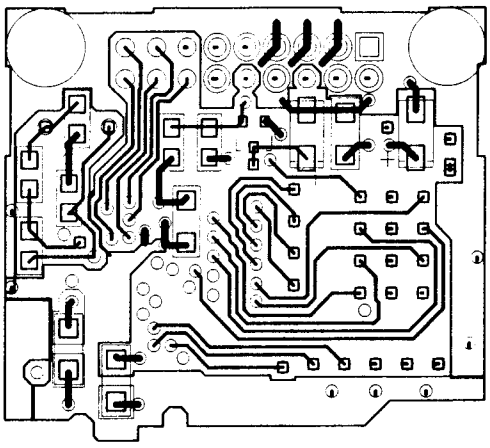
[2.8b] Other Design Examples w/ Neuron 3150 Chip

- **Core Circuit from TP/XF-1250 Control Module (4-layer, 10MHz device)**

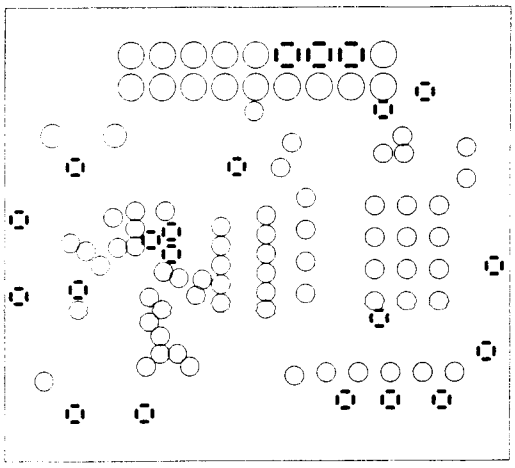
COMPONENT SIDE



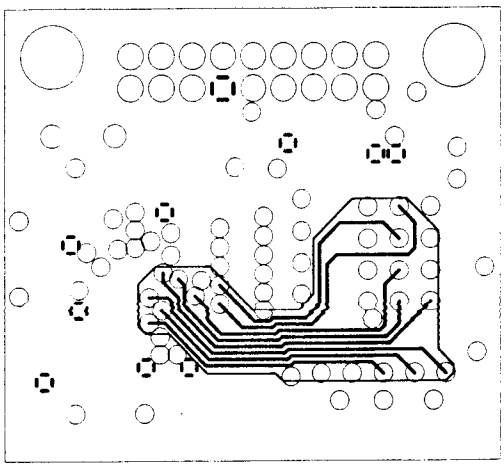
SOLDER SIDE



GROUND LAYER



VCC LAYER



[3] System Design Considerations

[3.1] ESD Hardening a Product Design

[3.2] EMI Management in a Product Design

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[3.1a] ESD Hardening a Product Design

- **First Strategy: Keep ESD arcs from entering the enclosure**
  - **Maintain long creepage distance from enclosure seams to internal circuitry**
- **If there are other entry points for ESD arcs into the device:**
  - **Use (uninsulated) chassis ground guards at entry points to capture the arcs before they can reach sensitive component leads**
  - **Shunt the arcs to star ground center as quickly as possible, without passing through sensitive circuitry**
  - **If circuitry is exposed to ESD arcs (LEDs, keyboard scanning traces, etc.), use diode clamps & Vcc decoupling cap to shunt ESD arc energy to ground, and route the arc current to the center of the star ground as soon as possible (see the keypad trace clamping example in Section 2.2 on star grounding)**
  - **All connectors that can return ESD arcs to chassis ground must be located together near the center of the star ground**

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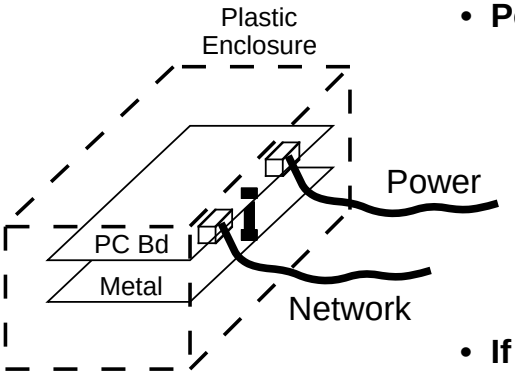
[3.1b] ESD Hardening a Product Design

- **Maintaining a Star Ground in a Plastic Package**
  - **Start with an understanding of where external metal objects will be in relation to your product**
    - Tabletop devices can sit on a metal table, or next to a metal file cabinet, etc.
    - Wall-mounted devices can be mounted next to metal studs, etc.



  - **Position a piece of metal (or metalized plastic) between your PC board and the external metal**
    - Tie the guard metal piece to the center of the PC board's star ground
    - Mechanically secure the guard metal to the package, or to the PC board with non-conducting standoffs of some kind
  - **If there is no external metal nearby, the separate guard metal may not be needed**

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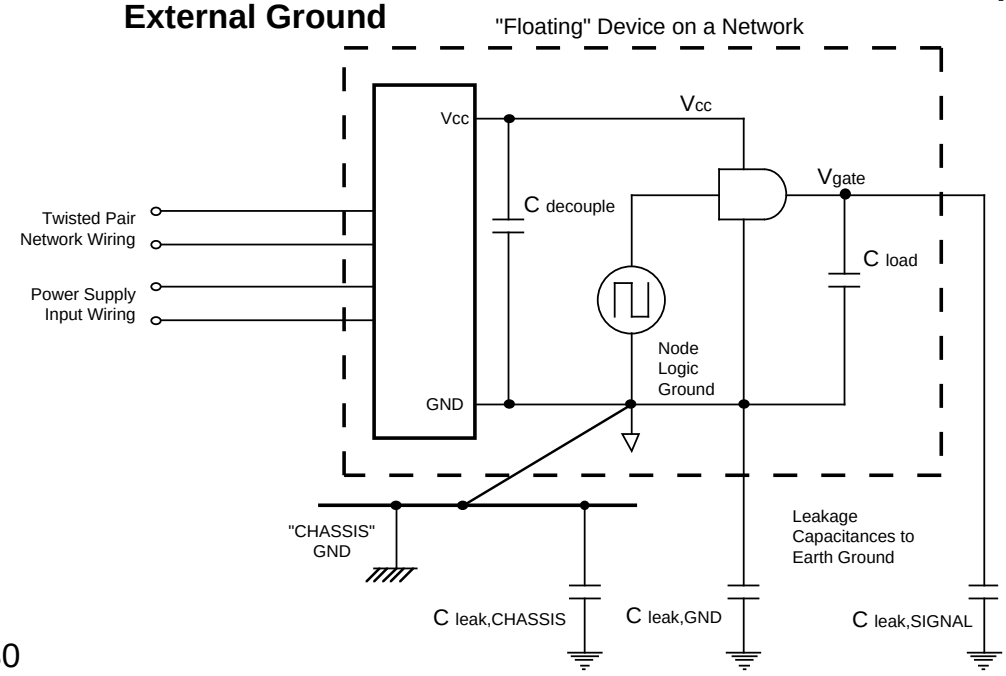
[3.2a] EMI Management in a Product Design

- **Stray Capacitance From Clock Lines To External Ground or Other Metal Surfaces Aggravates EMI**
- **Device Drives EMI Onto Network & Power Cables With Respect To External Ground**



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[3.2b] EMI Management in a Product Design

- **2nd Generation Neuron Chips Generate Less Vdd & CP Line noise (i.e.: 3150B1, 3120B1 Chips)**
  - For LONWORKS devices where the Neuron Chip's CP lines drive the network through a passive transceiver (like Direct Connect, TP/XF-78, TP/XF-1250), the quieter CP lines result in less EMI noise being driven onto the network cable
  - For LONWORKS devices that use an active transceiver (like PLT-xx, FTT-10, LPT-10), the quieter CP lines of the B1 chips will not directly lower EMI driven onto the network cable
    - The dominant noise source for devices with active transceivers is the RF noise on the Vcc pin of the transceiver
    - Active transceivers re-buffer the CP line signals, so it is transceiver noise, not Neuron Chip noise, that will be coupled onto the network cable
    - Trick: a little filtering on the Vcc pin of the active transceiver can lower EMI a lot (see Section 2.4 on decoupling)
- **TPT/XF Transceivers Make The Network Center Tap Available**
  - Tie this transformer center tap (network side) to external chassis metal if logic ground is isolated from chassis ground (use about 100pF; see the TPT User's Guide)

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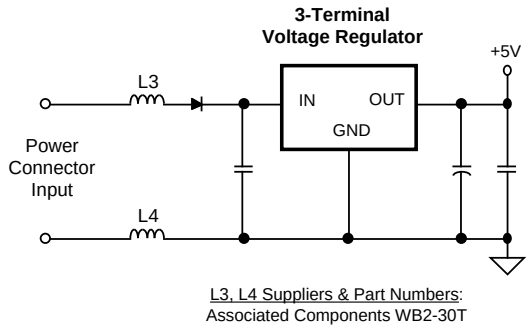
[3.2c] EMI Management in a Product Design

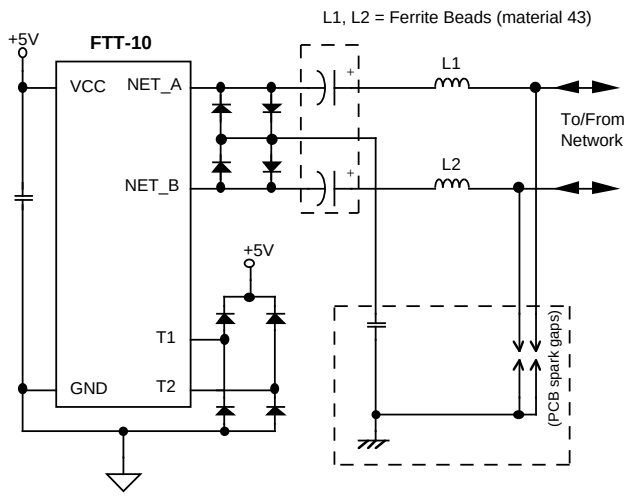
- **Ferrite Chokes Can Be Used When Desired For Additional EMI Margin**

Power Supply Input Chokes



L3, L4 Suppliers & Part Numbers:
Associated Components WB2-30T
Fairrite 2943666631

Ferrite Beads On Network Outputs



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[4] PCB Testing & Design Revisions

[4.1] General Test Strategy & Pass Crieteria

[4.2] STRIFE Testing

[4.3] IEC801-2 ESD Testing

[4.4] IEC801-3 RF Susceptibility Testing

[4.5] IEC801-4 Burst Testing

[4.6] IEC801-5 Surge Testing

[4.7] EMI Radiated & Conducted Emissions Testing

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[4.1] General Test Strategy & Pass Criteria

- **Best Initial Testing Strategy (depends on the application, of course):**
  - **Design a good Neuron C test program that is self-starting after resets, generates lots of network traffic, keeps statistics & info on failures, and has a visual indication of passing/failed**
  - **Assemble a representative test setup with several devices communicating over network cable**
  - **Test the first prototype PC board prototypes available (generally cannot test hand-wired prototype boards)**
  - **Start with Temperature testing, then STRIFE & ESD**
    - Debug any problems with these tests first, since they are the most fundamental & hardest to pass
  - **After initial STRIFE & ESD tests are passing, perform initial testing for Burst, Surge, EMI and RF Susceptibility**
  - **Perform the rest of your environmental test suite (humidity, supersoak, mechanical shock, vibration, altitude, etc.)**
  - **Final PC boards should be re-tested to verify full compliance (CE Mark certification may require independent lab testing)**
- **General Pass Criteria**
  - **For transient testing (ESD, Burst, Surge, etc.), it is generally okay to lose one network packet during the transient, but there should be no resets or loss of functionality**
  - **Some standards define various Performance Criteria Levels (see EN50082-1, for example)**

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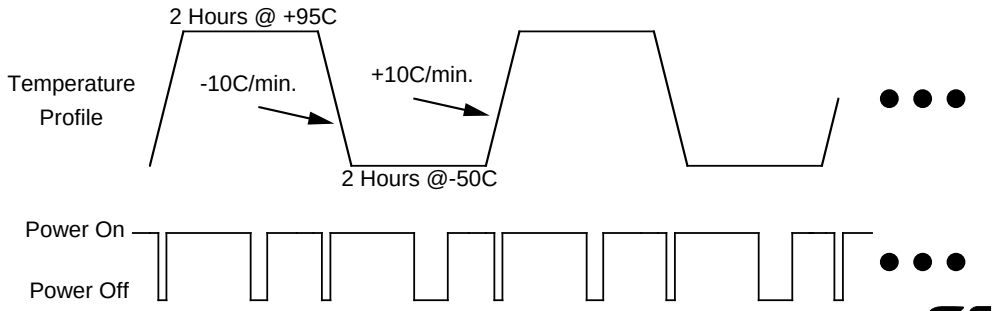
[4.2] STRIFE Testing

- **STRIFE = "Stressed Life" testing initially pioneered by HP San Diego**
- **Provides accelerated MTBF, reliability and margin testing**
- **Thermal stresses & power cycling are used together:**
  - For electrical assemblies, use ± 10C / minute thermal ramping
  - Motors, solenoids, etc., are generally limited to ± 5C / minute ramps
  - Temperature profile should extend 10C-15C beyond the operating temperature range of the product
- **Typical STRIFE profile used by Echelon to test a -40C to +85C device:**



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[4.3a] IEC801-2 ESD Testing

- **Test Setup:**
  - **Metal tabletop over metal ground plane on floor**
  - **Standard test generator: ±30kV air discharge, ±8kV contact discharge**
  - **Level 4 testing is up to ±15kV air discharge, ±8kV contact discharge**
- **Test & Debug Tips:**
  - **Keep a real-time log of your ESD test setups, experiments & results (you will perform hundreds of experiments in a typical ESD test session, and understanding the behavior is key to effective debug)**
  - **Map out where ESD currents are flowing for different entry & exit points, and verify that the star ground layout of the PC board is keeping those currents away from any sensitive circuitry**
  - **Use the "Top Hat" rework to understand if better grounding & decoupling can help your ESD performance**
  - **If you need to observe any signals on your device while testing, the only option is a fiber optic probe**

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[4.3b] IEC801-2 ESD Testing

"Top Hat" Rework For The Neuron Chip

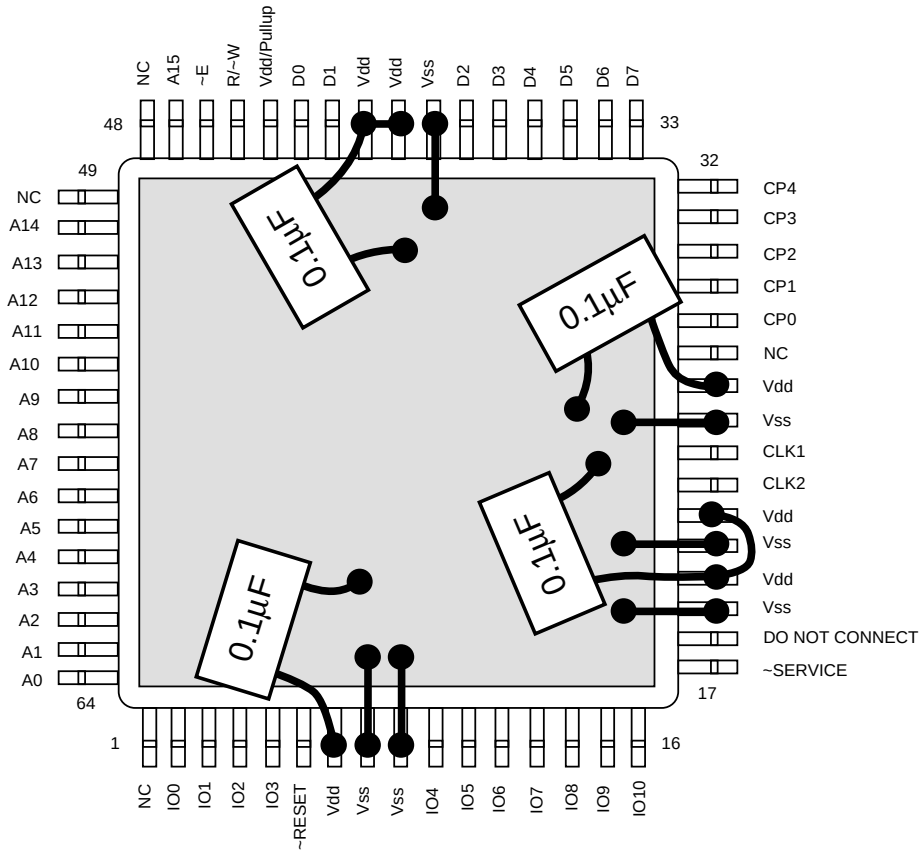
- **Extremely Effective Technique for ESD & EMI Debugging**
- **Rework Simulates Very Good Grounding & Decoupling on The PCB**
- **Rework Steps (Neuron 3150 Chip Shown):**

1) Cut a square of copper tape to cover the top of the Neuron Chip. This "Top Hat" forms an accessible ground plane on top of the chip.

2) Using thin wire (i.e. bare wire-wrap wire), connect each Vss pin to the top hat ground plane. Keep the wire connections as short as possible.

3) Connect four 0.1µF ceramic radial caps as shown between the Vdd pins and the top hat ground plane. Keep all leads short.

4) If the PCB grounding to external memory devices is not low impedance, perform the same kind of top hat rework on the memory devices, and connect the top hat ground planes with a 0.5" wide strip of copper tape.



NEURON 3150 CHIP

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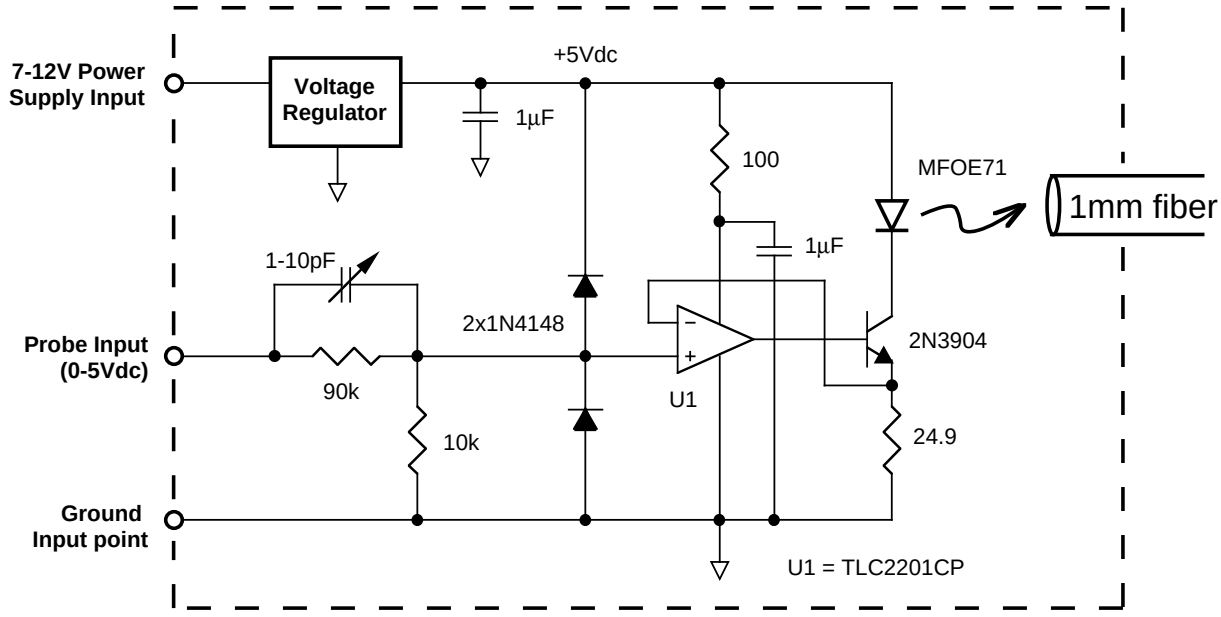
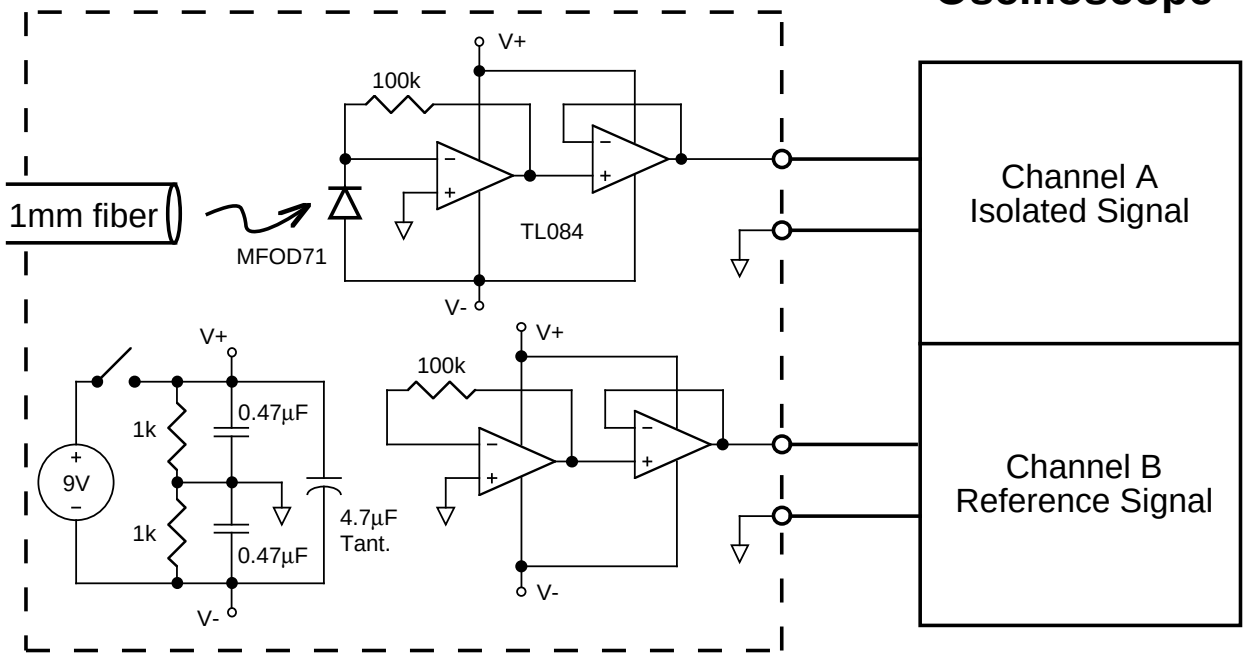
[4.3c] IEC801-2 ESD Testing

200kHz Fiber Optic Probe For Isolated Measurements



200kHz Fiber Optic Receiver

Battery-Powered Oscilloscope



- **(Note: a 20MHz Fiber Optic Probe can be built using a modified circuit, and HFBR-1526/2526 parts from HP.)**

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[4.4] IEC801-3 RF Susceptibility Testing

- **Test Setup:**
  - **RF transmitting antenna in an RF-shielded Anechoic chamber creates an intense electromagnetic field at the test table**
  - **RF transmitter is slowly swept from 27MHz to 500MHz (new revisions of this standard may change the frequency range)**
  - **The RF field is amplitude modulated with 1kHz sine wave, 80% AM**
  - **Level 3 testing is performed with Erms = 10V/m ("Severe Environment")**
- **Test & Debug Tips:**
  - **Ensure that transceivers, terminators, etc. are designed with as much symmetry as possible. Avoid any asymmetries that could lead to common mode to differential mode conversion of the RF signal. The network wiring will pick up several volts of RF signal (common mode), depending on frequency & test level.**
  - **Because of the severe electromagnetic field in the chamber during this testing, any circuit probing for debug purposes must be done using a fiber optic probe**

[4.5] IEC801-4 Burst Testing

- **Test Setup:**
  - **Network Cable Clamp Method: network cable is clamped in a one meter long test fixture, and burst noise is coupled into the network cable capacitively by the clamp. Level 4 testing with the cable clamp method uses ±2kV bursts ("Severe Industrial Environment").**
  - **Power Cord Coupling Method: the product's power cord is plugged into the test generator, and burst noise is coupled in various modes into the power cable. Level 4 testing with the power cord method uses ±4kV bursts.**
- **Test & Debug Tips:**
  - **Star grounding is very important in this testing, so be sure to trace out the path that transient currents will take from the network cable and power cable to chassis ground**
  - **Because of the large voltage "bounces" generated during burst testing, a fiber optic probe must be used if circuitry is probed for debugging**

[4.6] IEC801-5 Surge Testing

- **Test Setup:**
  - **Surge testing is performed using a specialized test generator**
  - **The surge waveforms are coupled directly onto the network cable via a coupling circuit (see the 801-5 specification)**
  - **Level 3 testing is performed with up to ±2kV surges.**
- **Test & Debug Tips:**
  - **The energy involved in surge testing is much greater than either ESD or burst testing. This extra energy stresses transient-absorbing components, so be sure to check the power ratings of any explicit transient suppressors that you are using**
  - **This extra energy makes surge testing a serious shock hazard, and components that fail in surge testing often do so violently.... Be careful, and always wear your safety glasses while involved in this testing**

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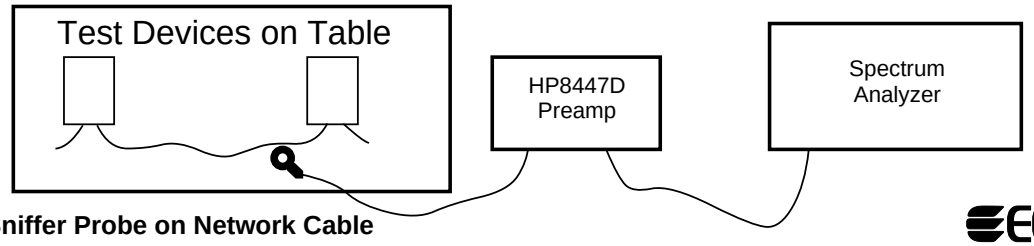
[4.7a] EMI Radiated & Conducted Testing

- **Test Setup:**
  - **Outdoor EMI test range is used for final testing & absolute level checks**
  - **Indoor testing is more convenient for debug & experiments. Indoor testing can be performed in an RF-shielded screen room using antennas, or it can be performed using sniffer probes (see below)**
  - **Level "A" limits generally apply to industrial equipment, and the more stringent level "B" limits apply to residential equipment.**
- **Test & Debug Tips:**
  - **Use sniffer probes to trace out near-field magnetic noise to help map where RF currents are flowing in cables & packaging**
  - **Use indoor test setup with a sniffer probe on the network cable to perform convenient experiments, then use outdoor EMI scan data to correlate cable scans with absolute EMI levels**



Sniffer Probe on Network Cable

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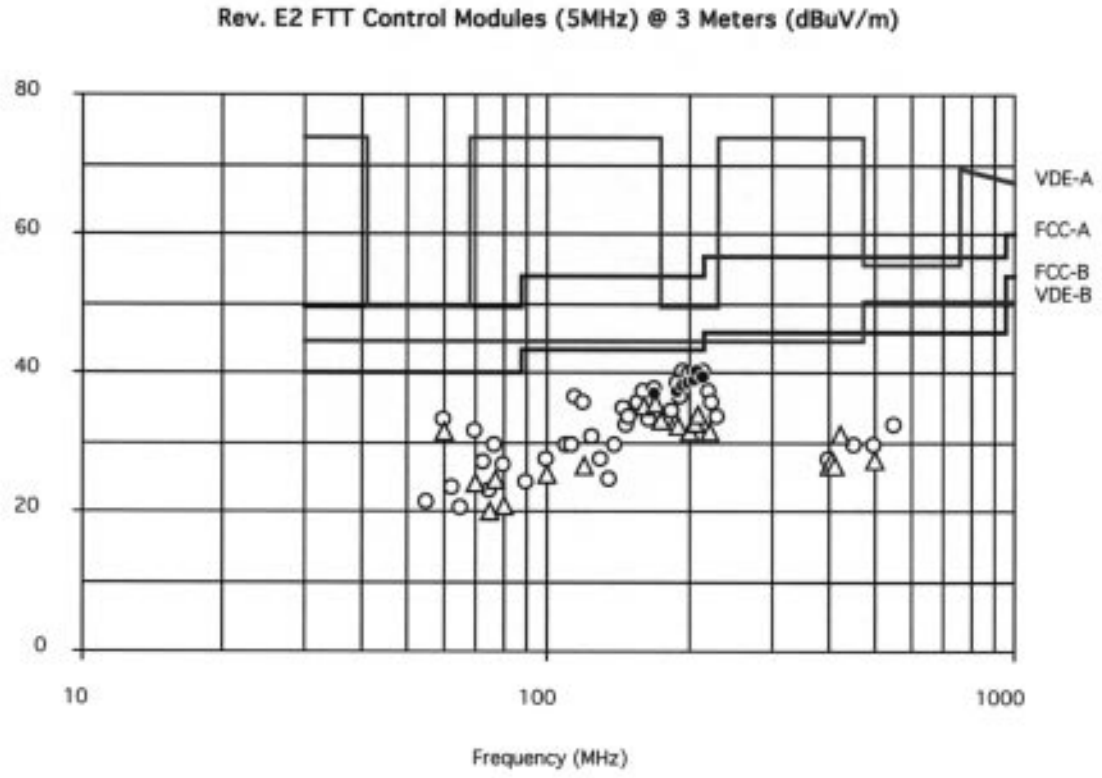
[4.7d] EMI Radiated & Conducted Testing

EMI Radiated Plot Taken From Recent Echelon Testing:

- **Multiple TP/FT-10 Control Modules In Router Bases (no tops)**
- **Network Cable Lengths Resonant Around 200MHz**
- **ANSI C63.4 Setup, MP4 Test Procedure Used (to maximize the EMI & look for any potential problems)**



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[5] References, Suggested Reading & Suppliers

- **References & Suggested Reading**
  - EDN Designer's Guide to Electromagnetic Compatibility, EDN Supplement, 1/20/94. Available from EDN (call 800-523-9654).
  - Noise Reduction Techniques in Electronic Systems, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.
  - Protection of Electronic Circuits from Overvoltages, by Ronald B. Standler, John Wiley & Sons, 1989.
  - High-Speed Digital Design, by Howard W. Johnson and Martin Graham, Prentice Hall, 1993.
  - Interference Technology Engineer's Master (ITEM), Resource Directory for EMC Products & Services, published by R&B Enterprises (call 610-825-1960).

- **Some Suppliers Used By Echelon**
  - EMI Sniffer Probe Kit: EMCO Model 7405 (call 512-835-4684).
  - Fiber Optic (200kHz Analog) Parts: Motorola MFOE-71, MFOD-71.
  - Fiber Optic (50MHz Analog) Parts: HP HFBR-1526, HFBR-2526.
  - Environmental Test Lab: Continental Viking Labs (call 415-969-5500).
  - EMI & IEC Testing: C&C Labs (call 510-440-3838).
  - EMI & Safety Testing: Elliot Labs (call 415-967-4166).

- **Acknowledgements**

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  - Thanks to Mr. Dana Craig (an EMI consultant here in Silicon Valley), for his invaluable help in Echelon's EMI compliance work.
  - Thanks to Mr. Ed Nordquist (a PC Board designer here in Silicon Valley), for his patience and understanding while enduring multiple revisions of our PC boards to tune EMI and ESD performance.

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